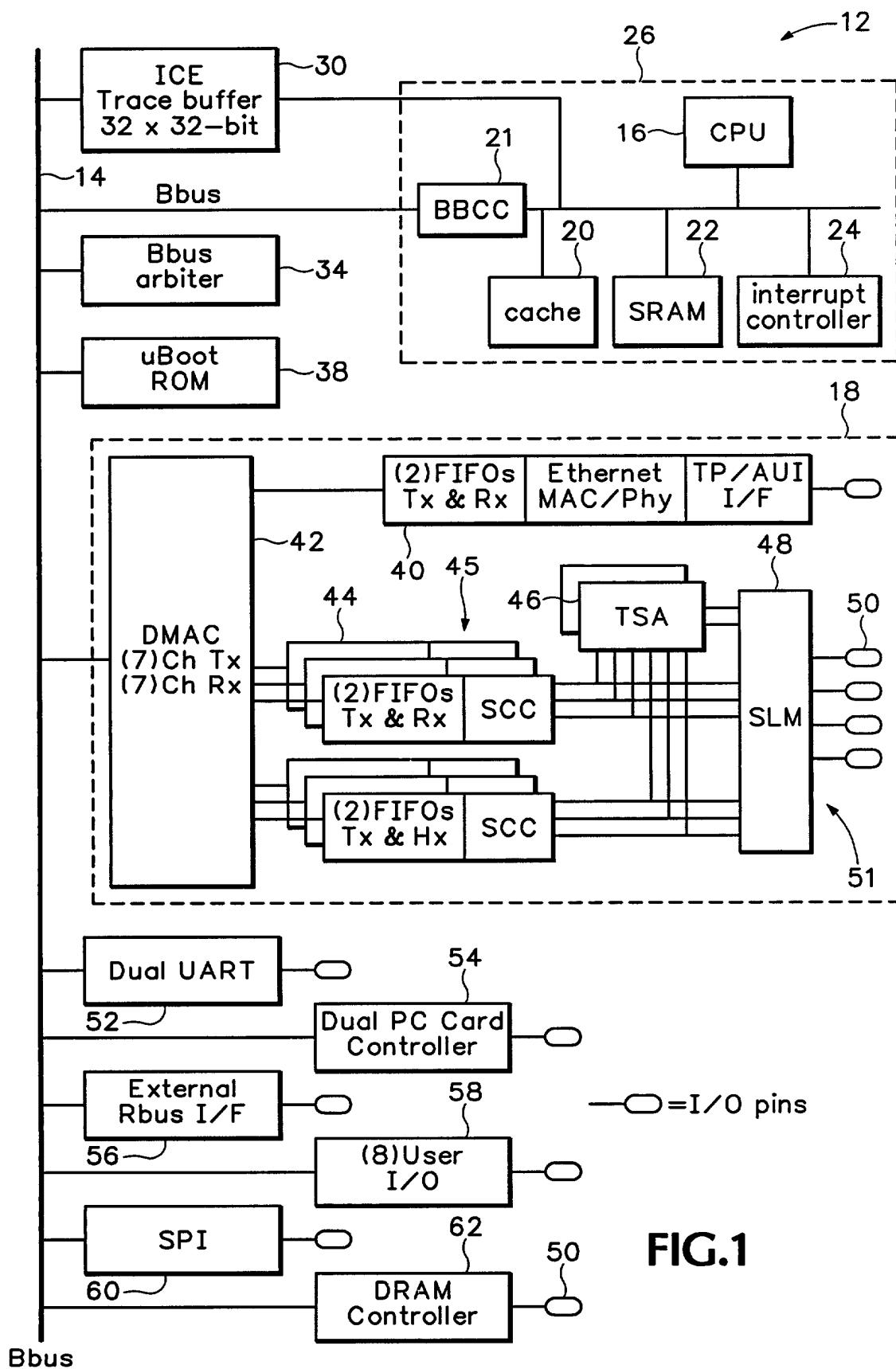


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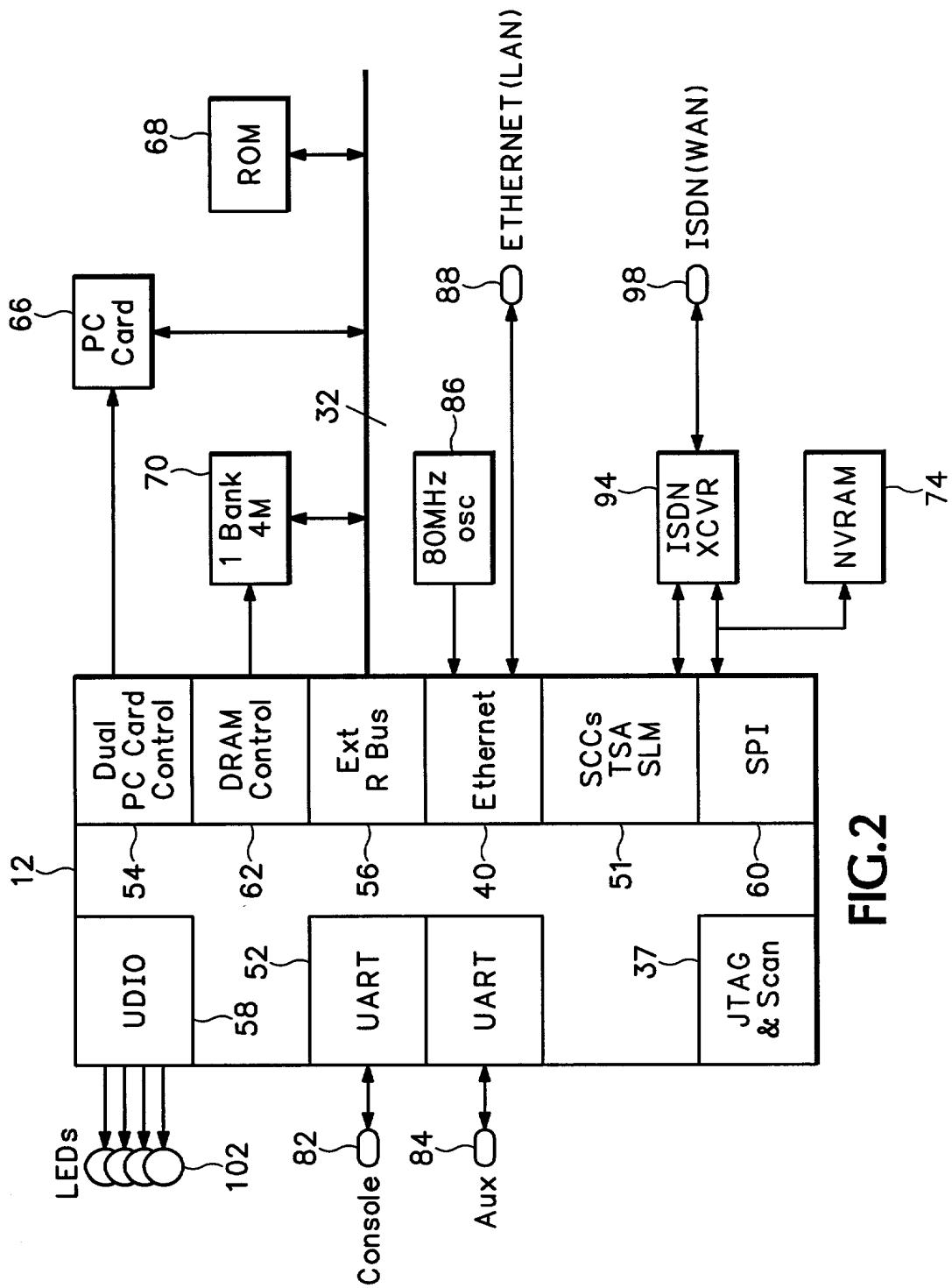


FIG.2

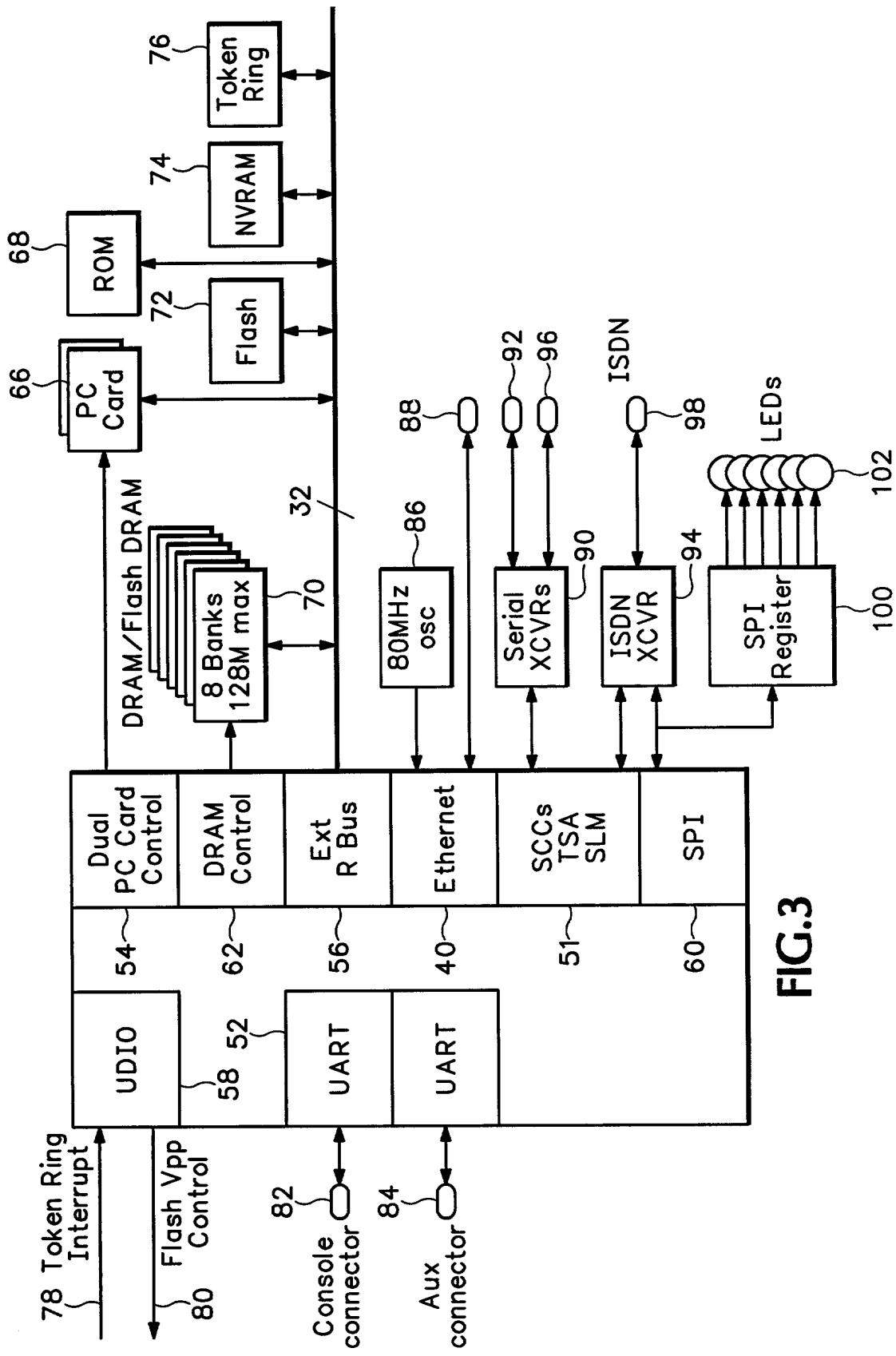


FIG.3

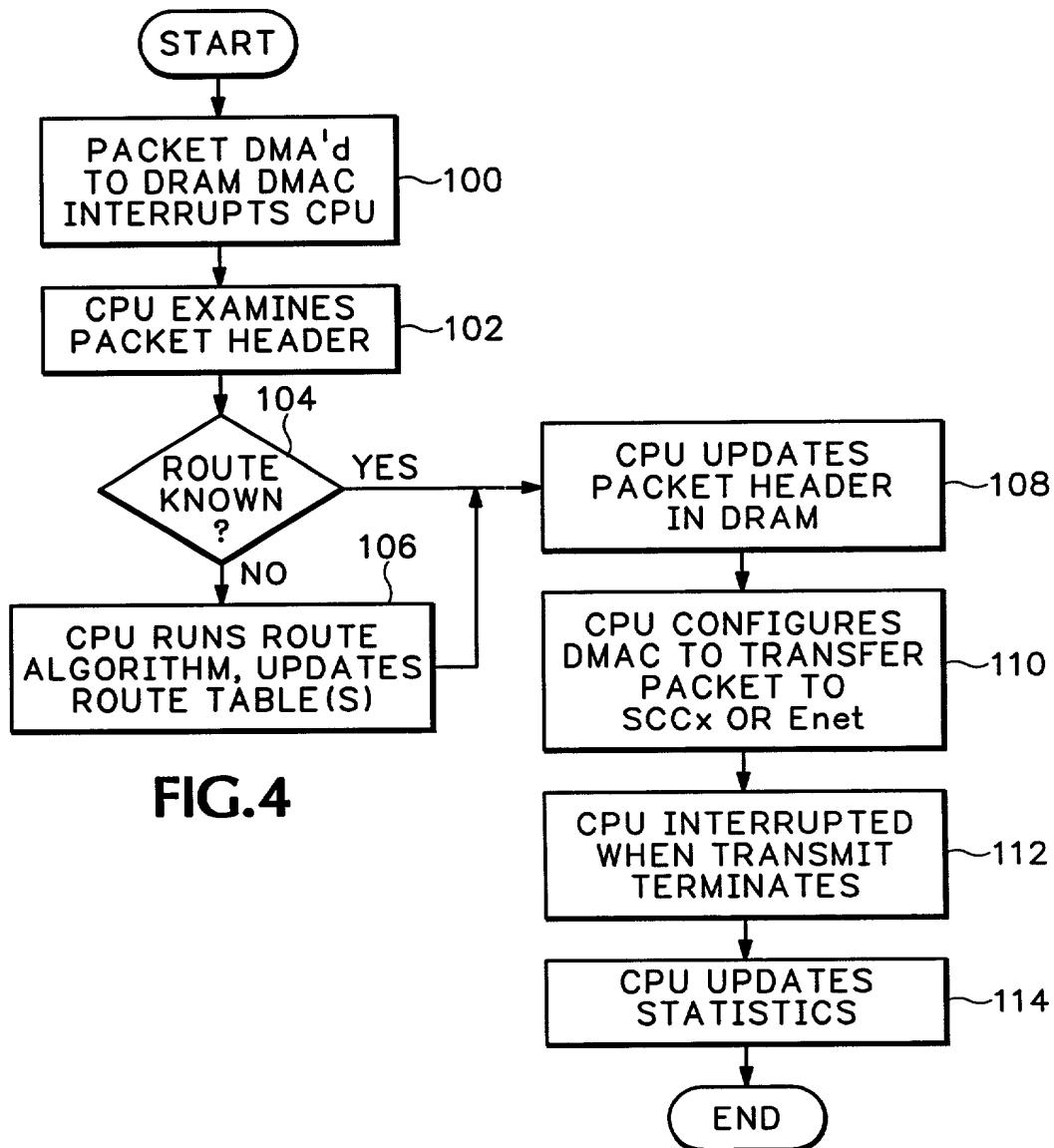


FIG.4

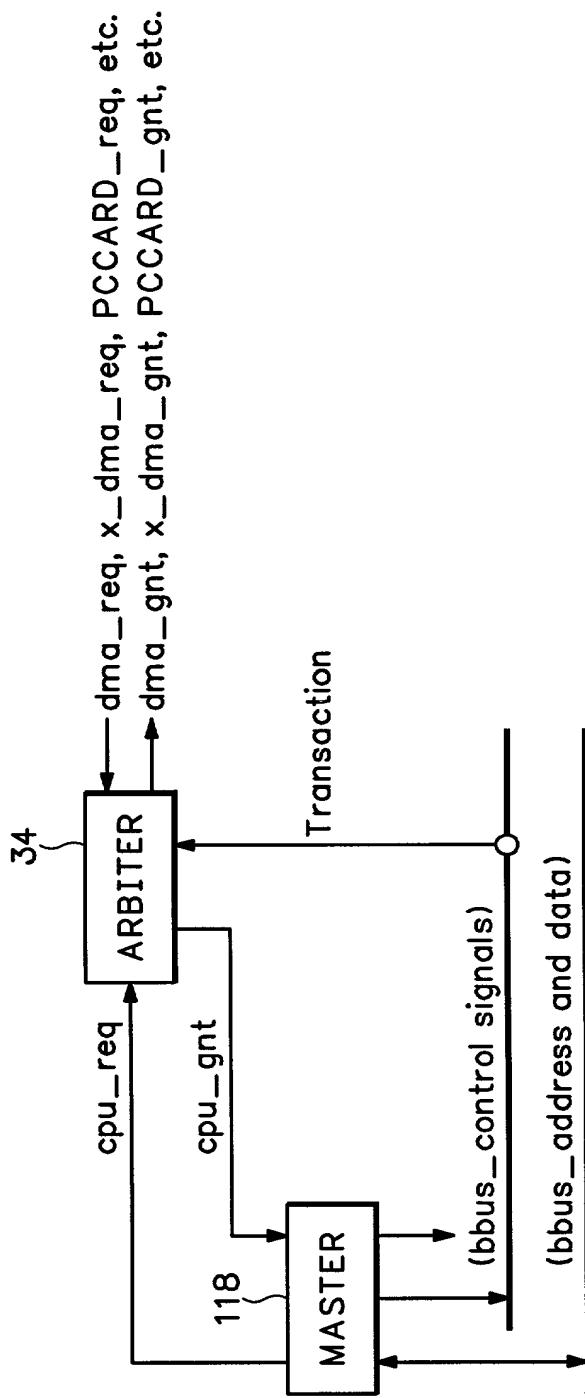


FIG.5
MODULE INTERFACE

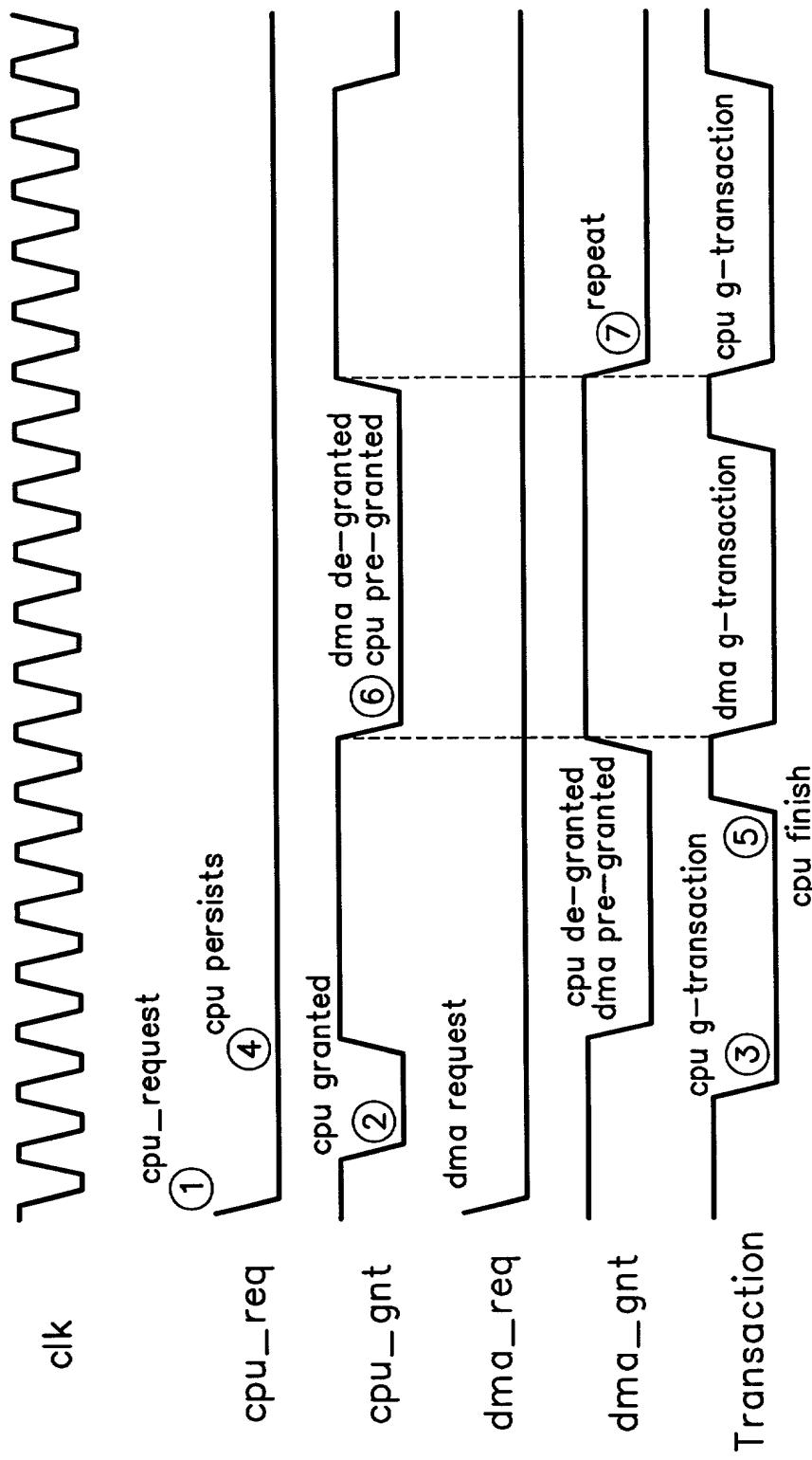


FIG.6
PIPELINED ARBITRATION
PROTOCOL EXAMPLE

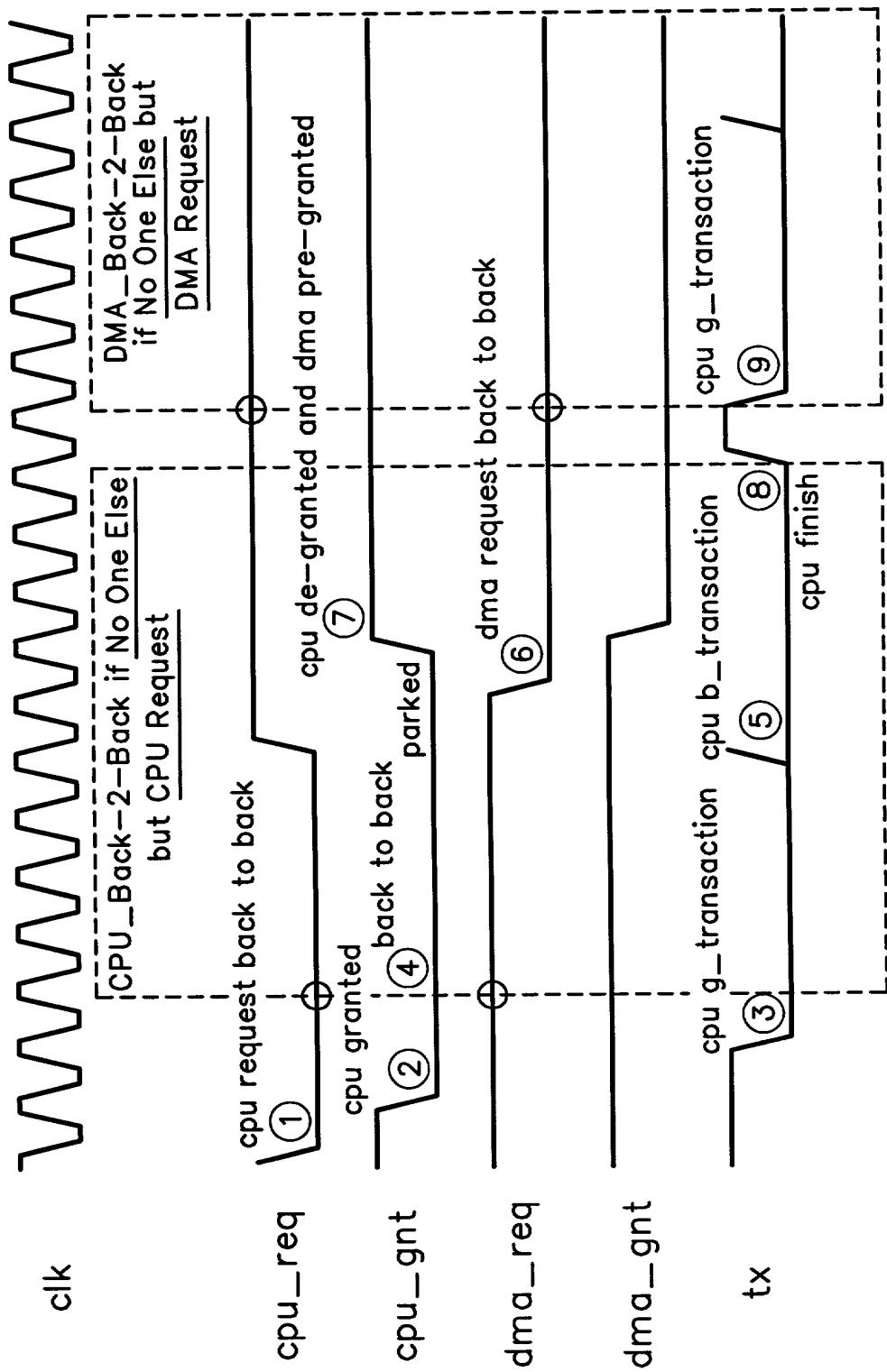


FIG.7
ARBITRATION PROTOCOL EXAMPLE
BACK-TO-BACK TRANSACTION

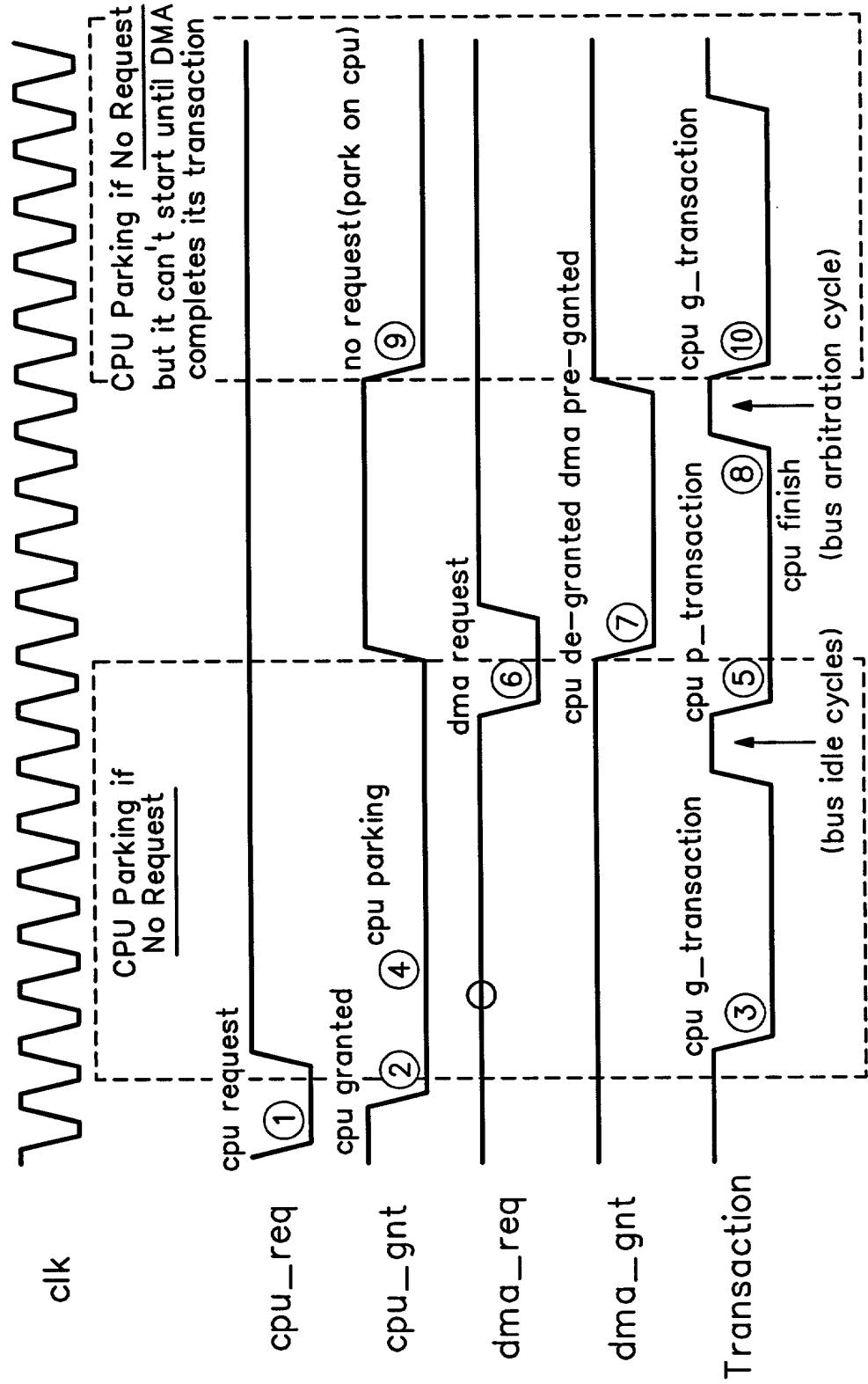


FIG. 8
ARBITRATION PROTOCOL EXAMPLE
PARKING

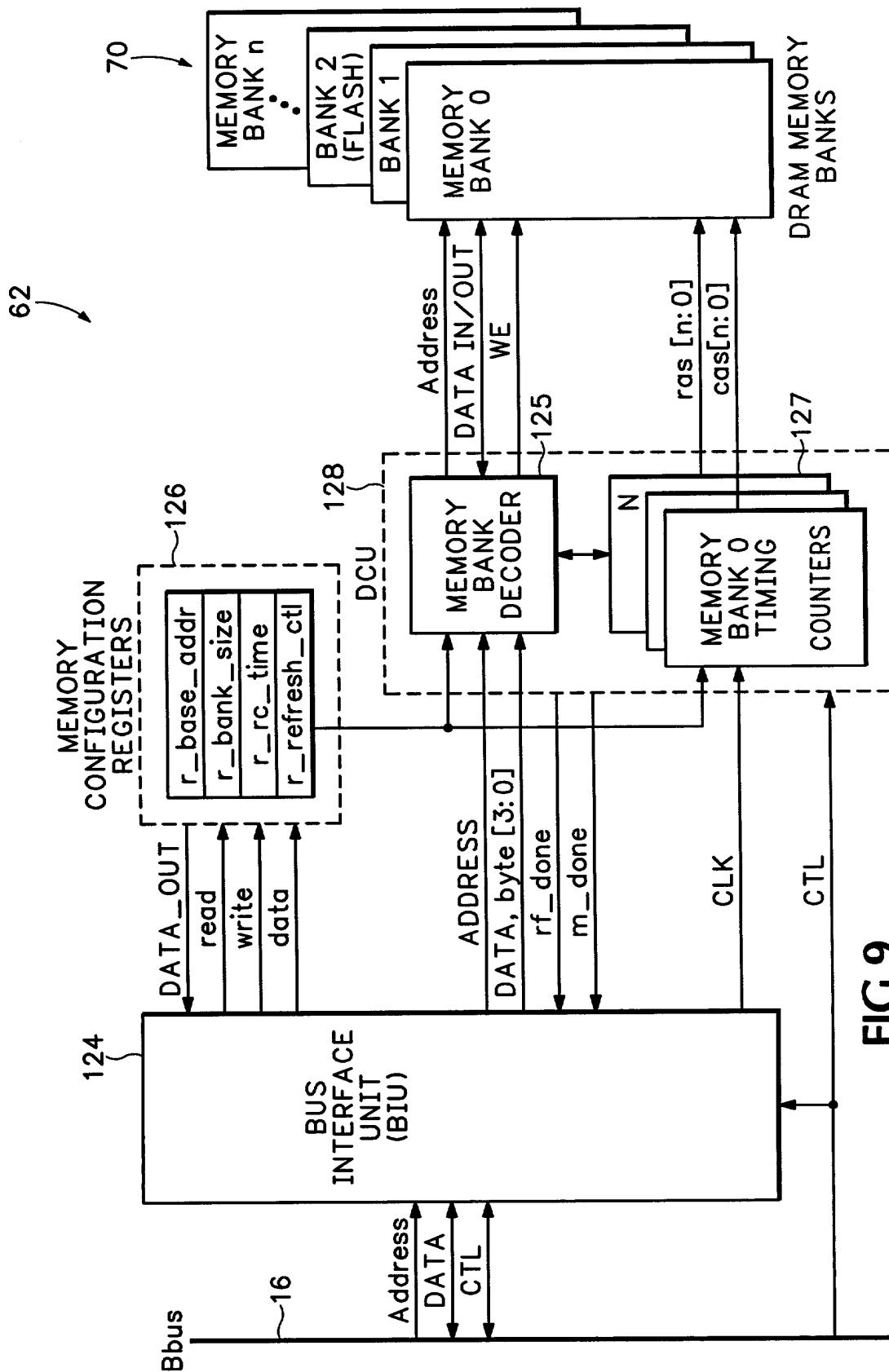
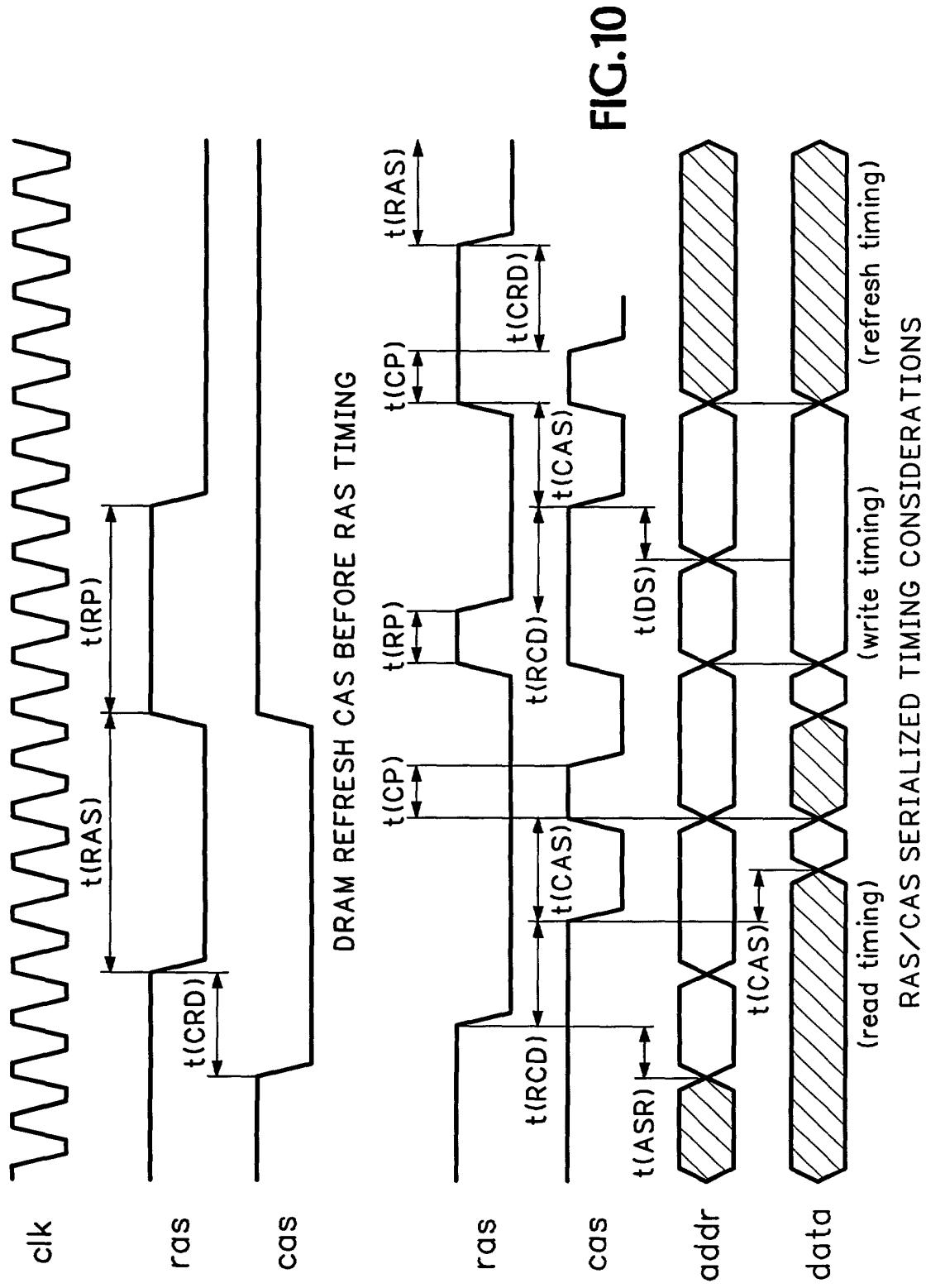


FIG.9
DRAM CONTROLLER



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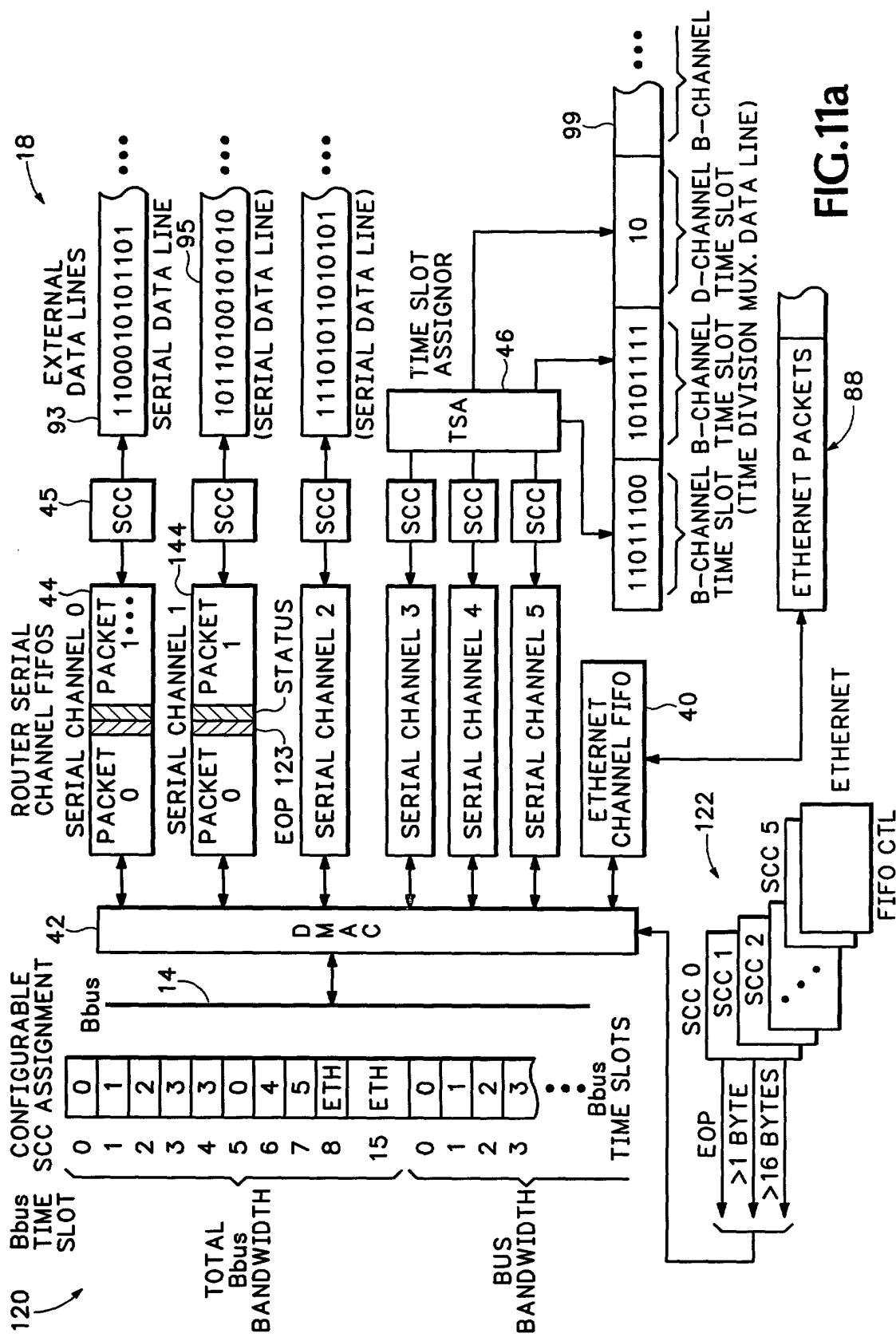
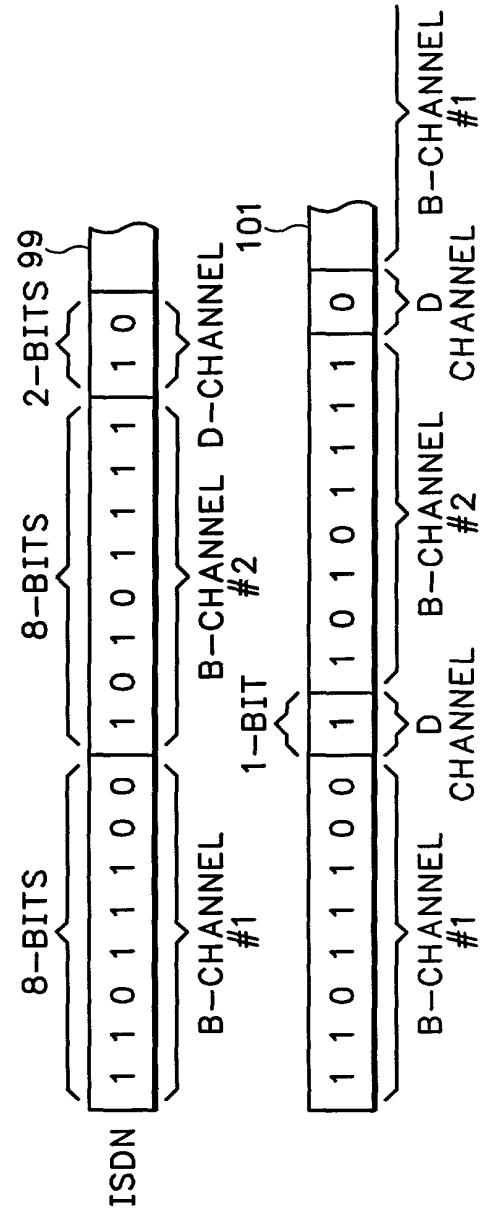
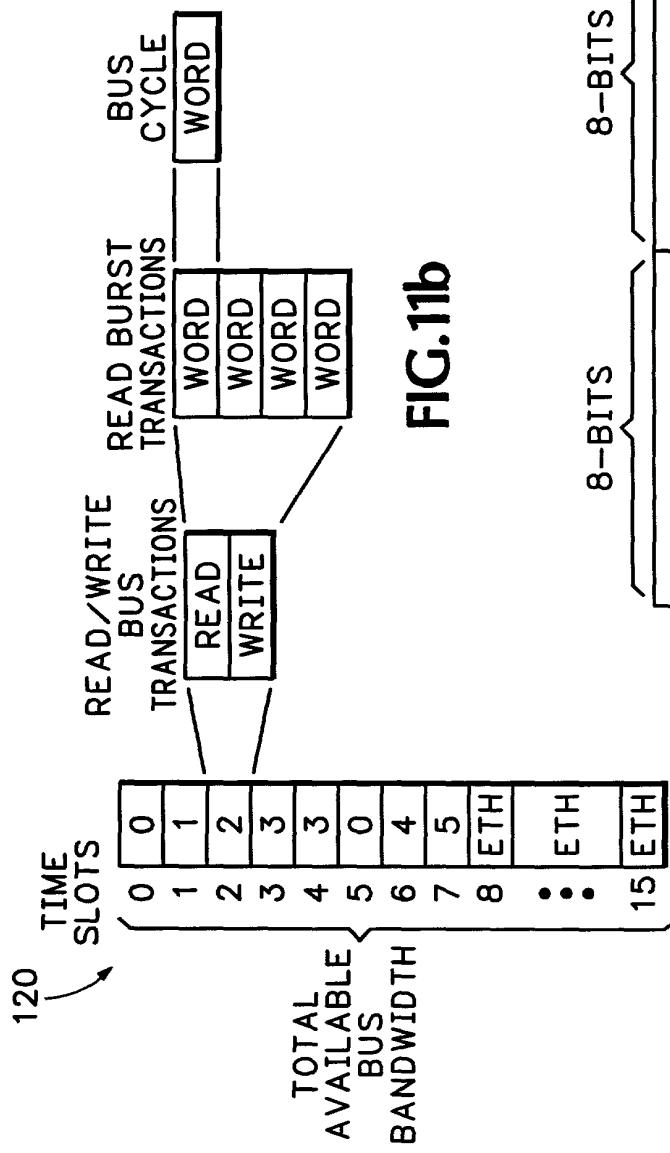


FIG.11a



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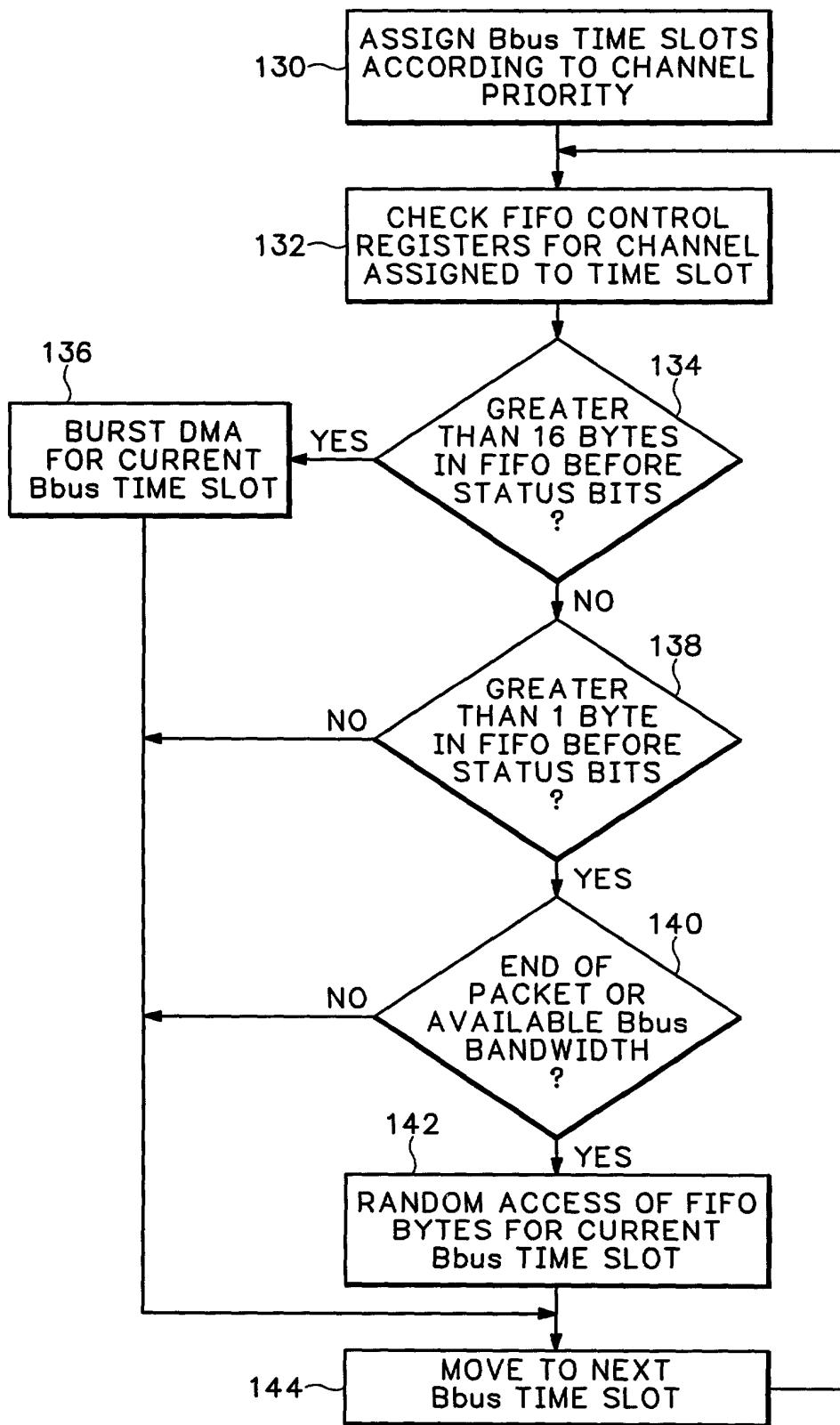


FIG.13

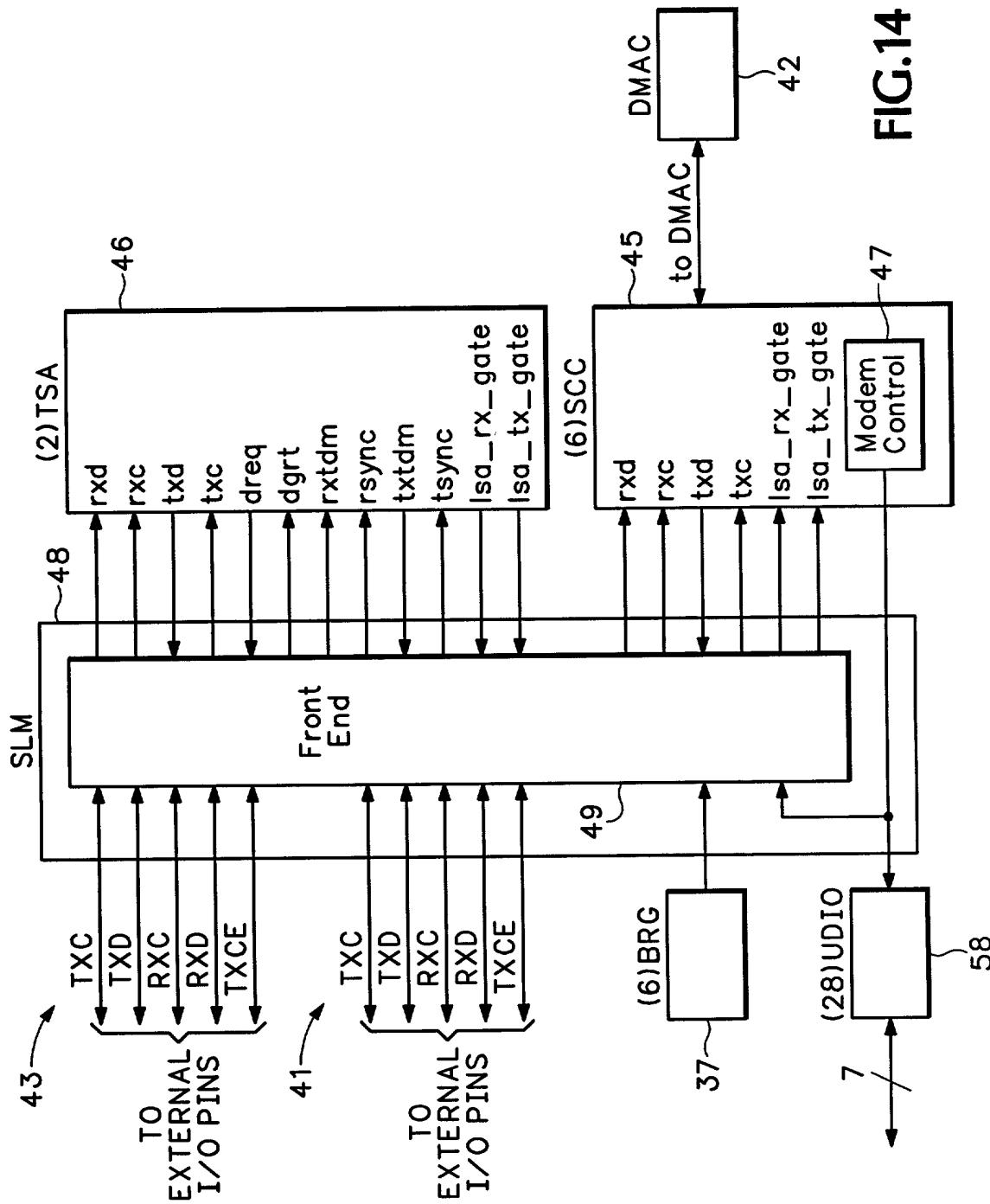


FIG.14

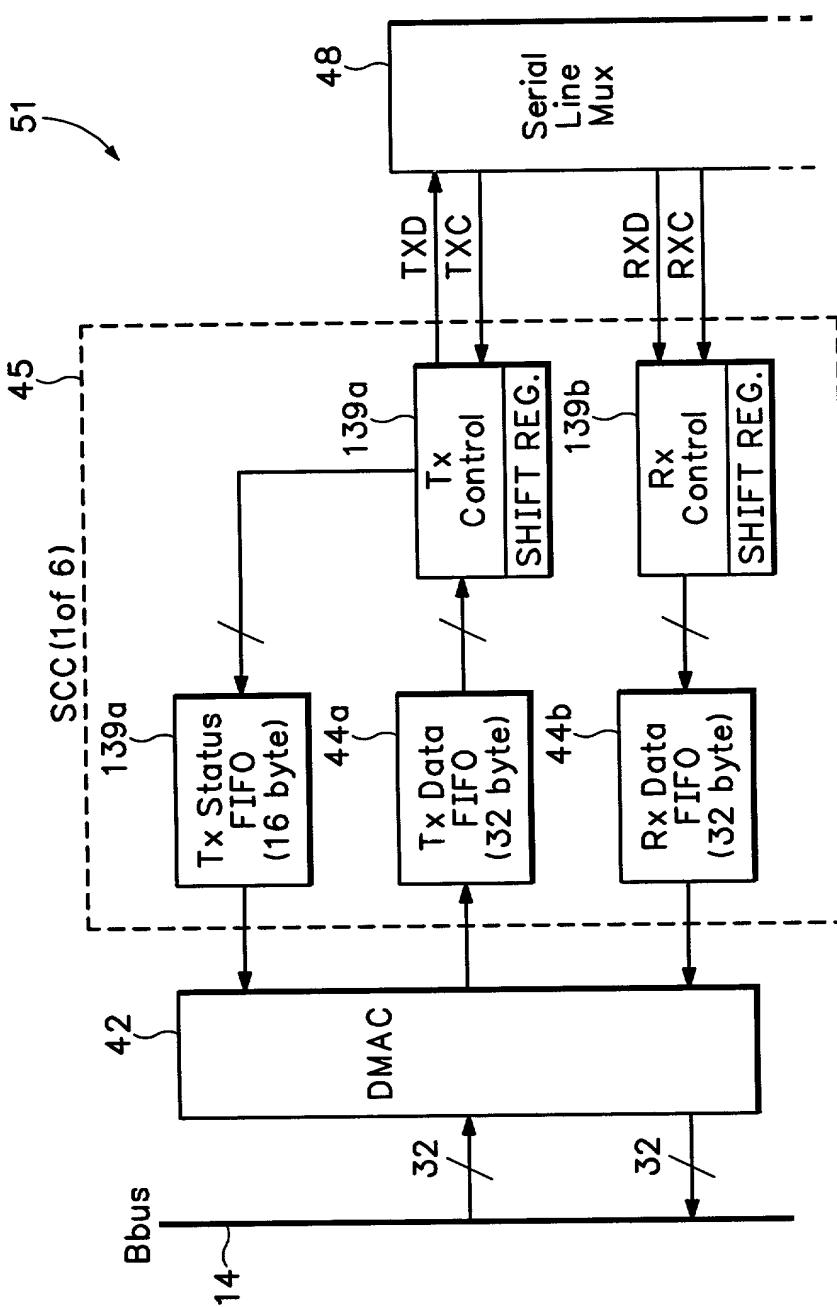


FIG.15

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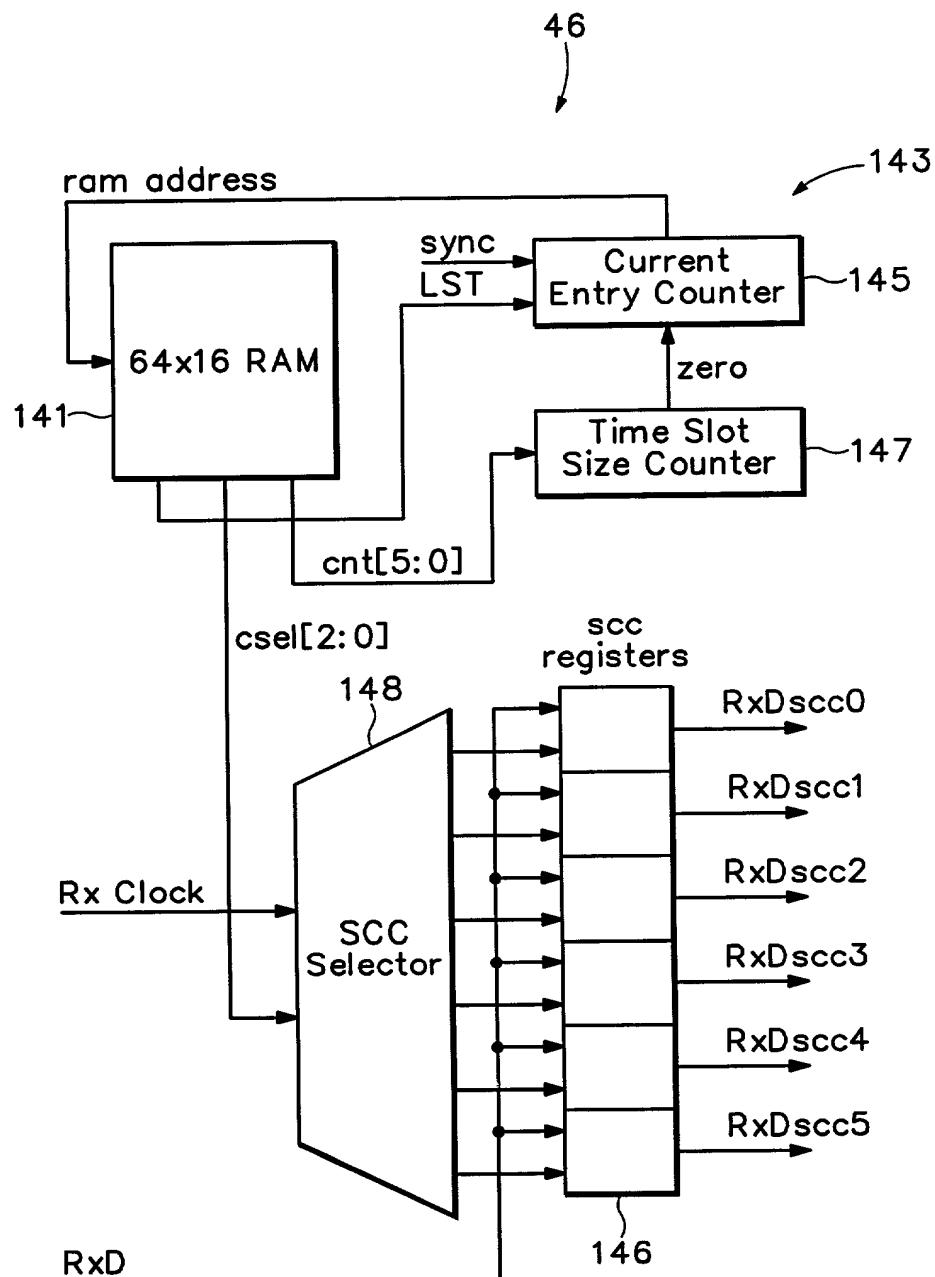


FIG.16
TSA RECEIVE
BLOCK DIAGRAM

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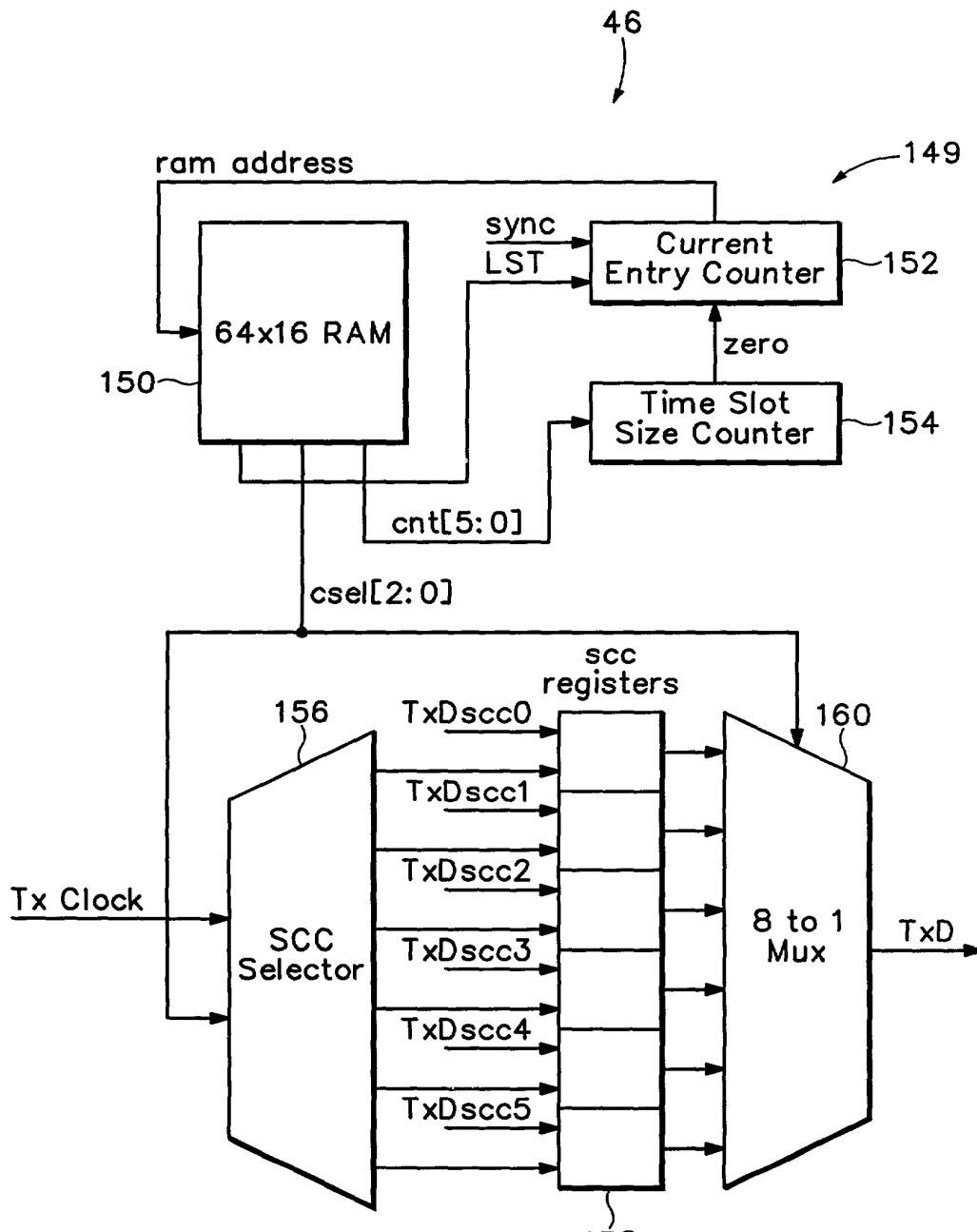


FIG. 17

TSA TRANSMIT
BLOCK DIAGRAM

15	14	13	12	11	10	9	8	6	5	162	0
SKIP	0	BYT	XTR	LST	0	0	CSEL			CNT	

FIG. 18

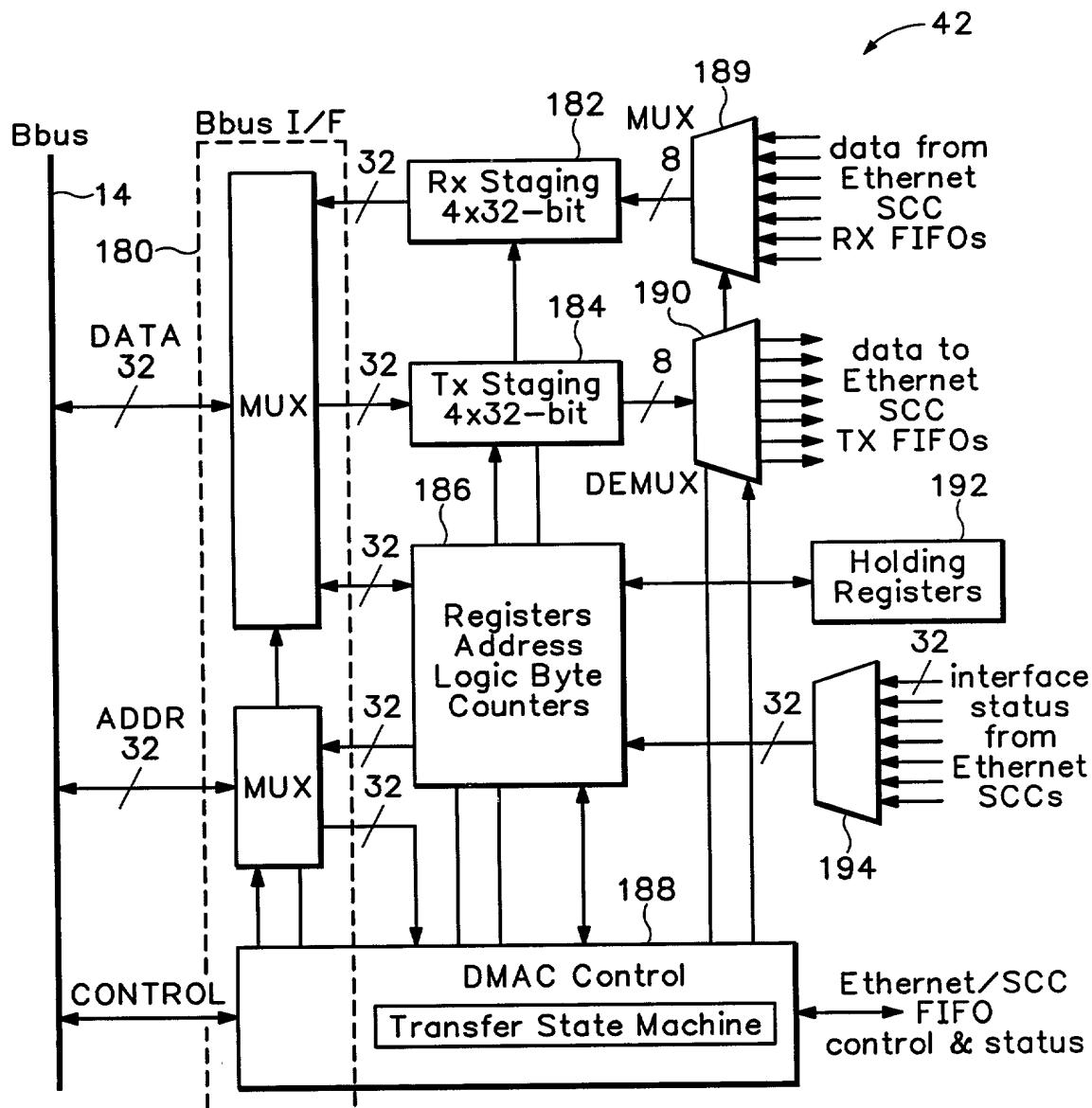


FIG.19
DMAC BLOCK DIAGRAM

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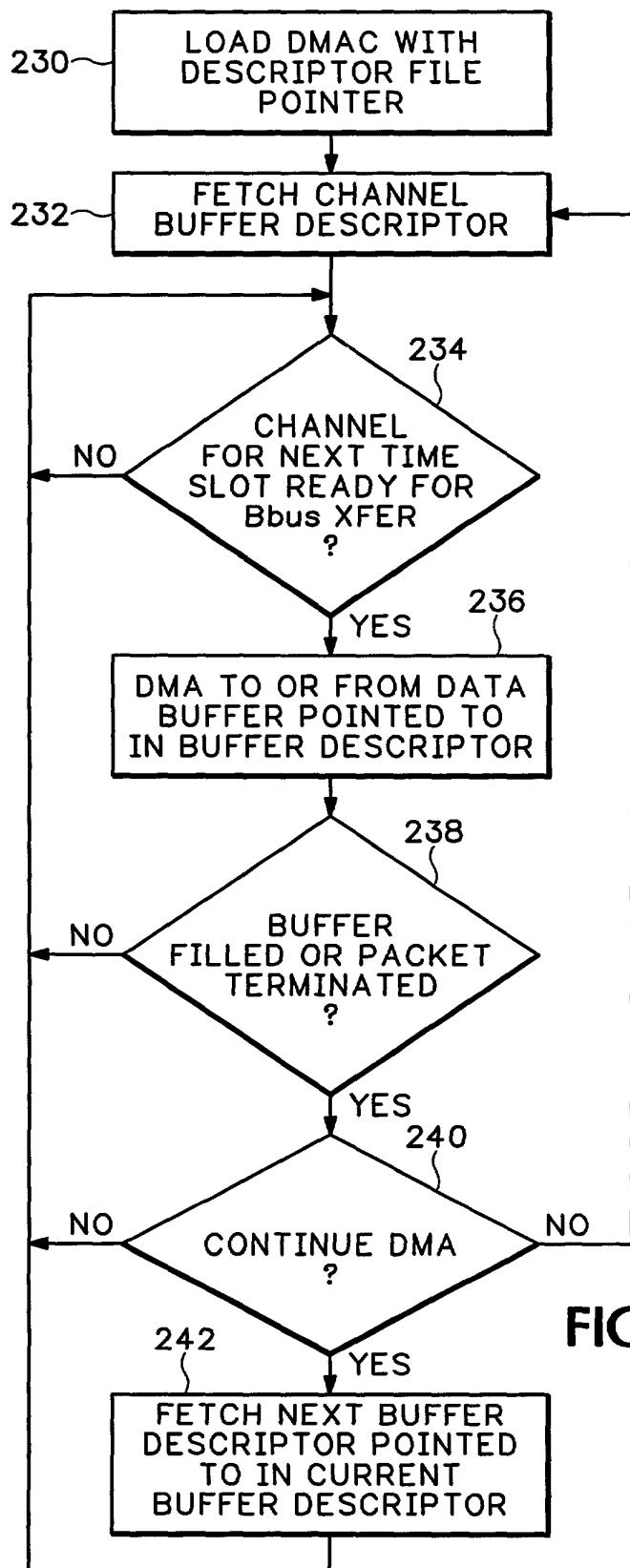


FIG.20

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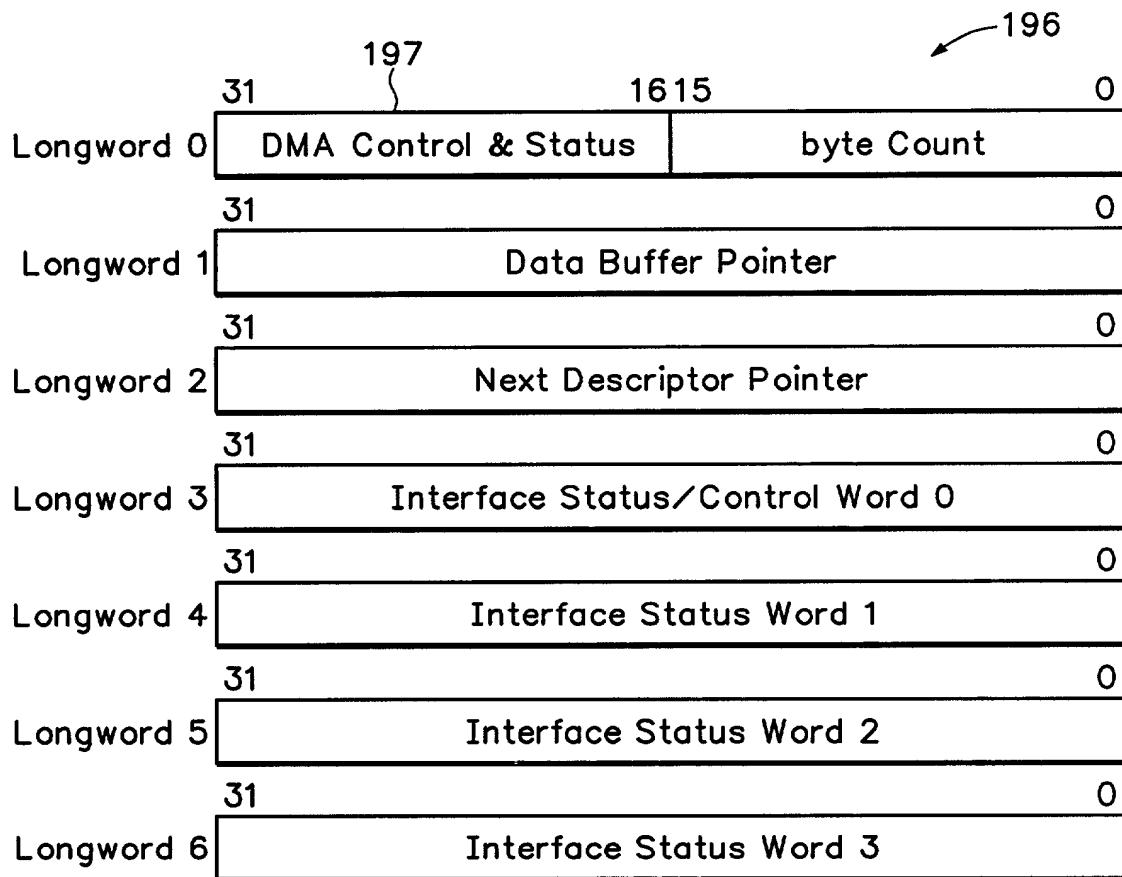


FIG.21
BUFFER DESCRIPTOR

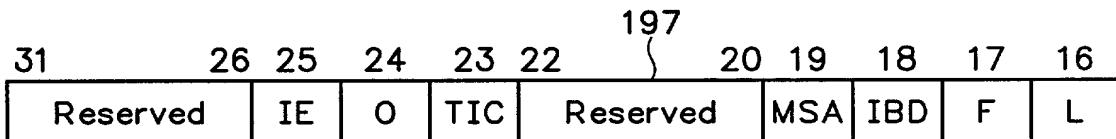


FIG.22
DMA CONTROL & STATUS
FIELD OF DESCRIPTOR

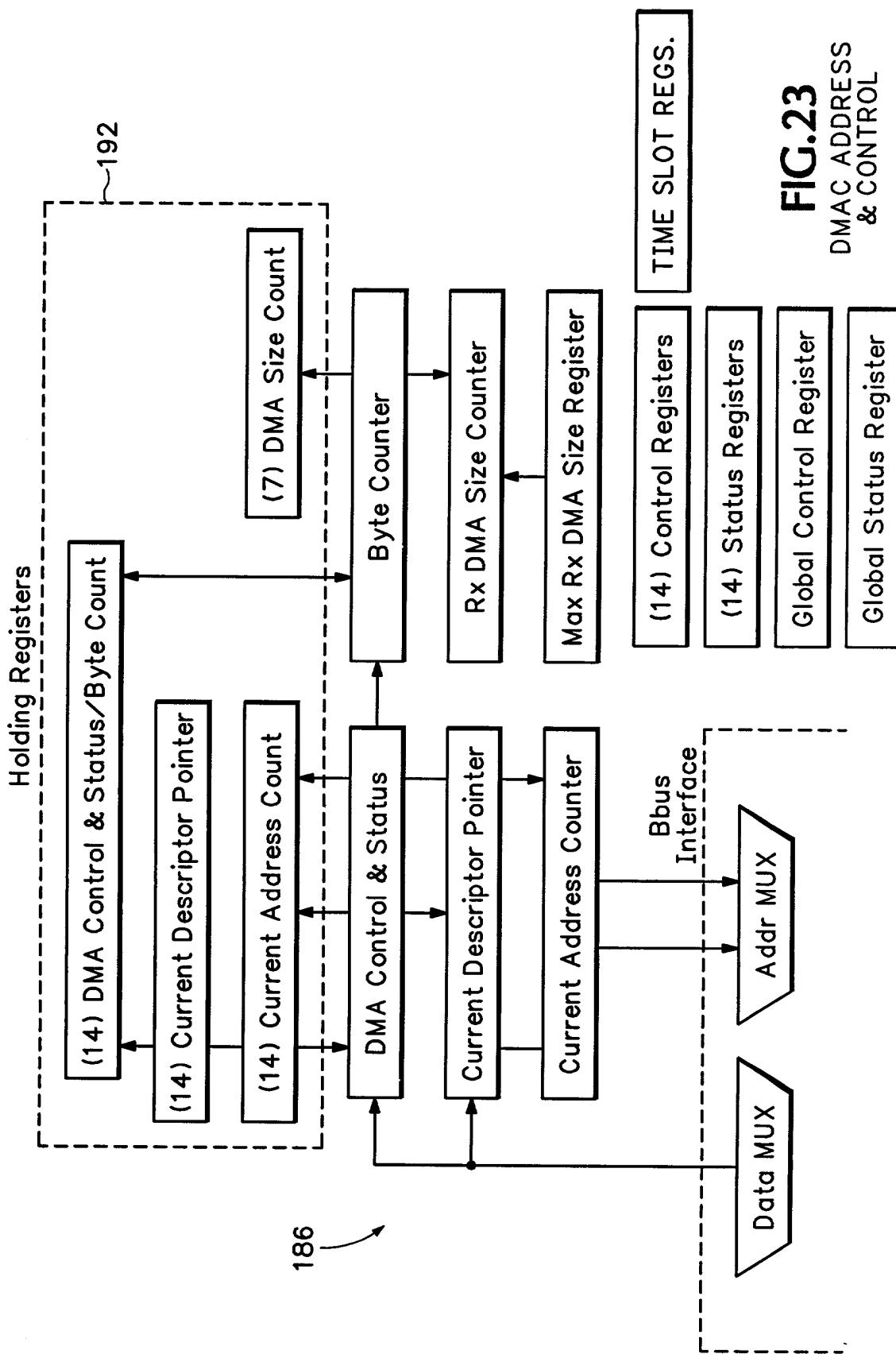
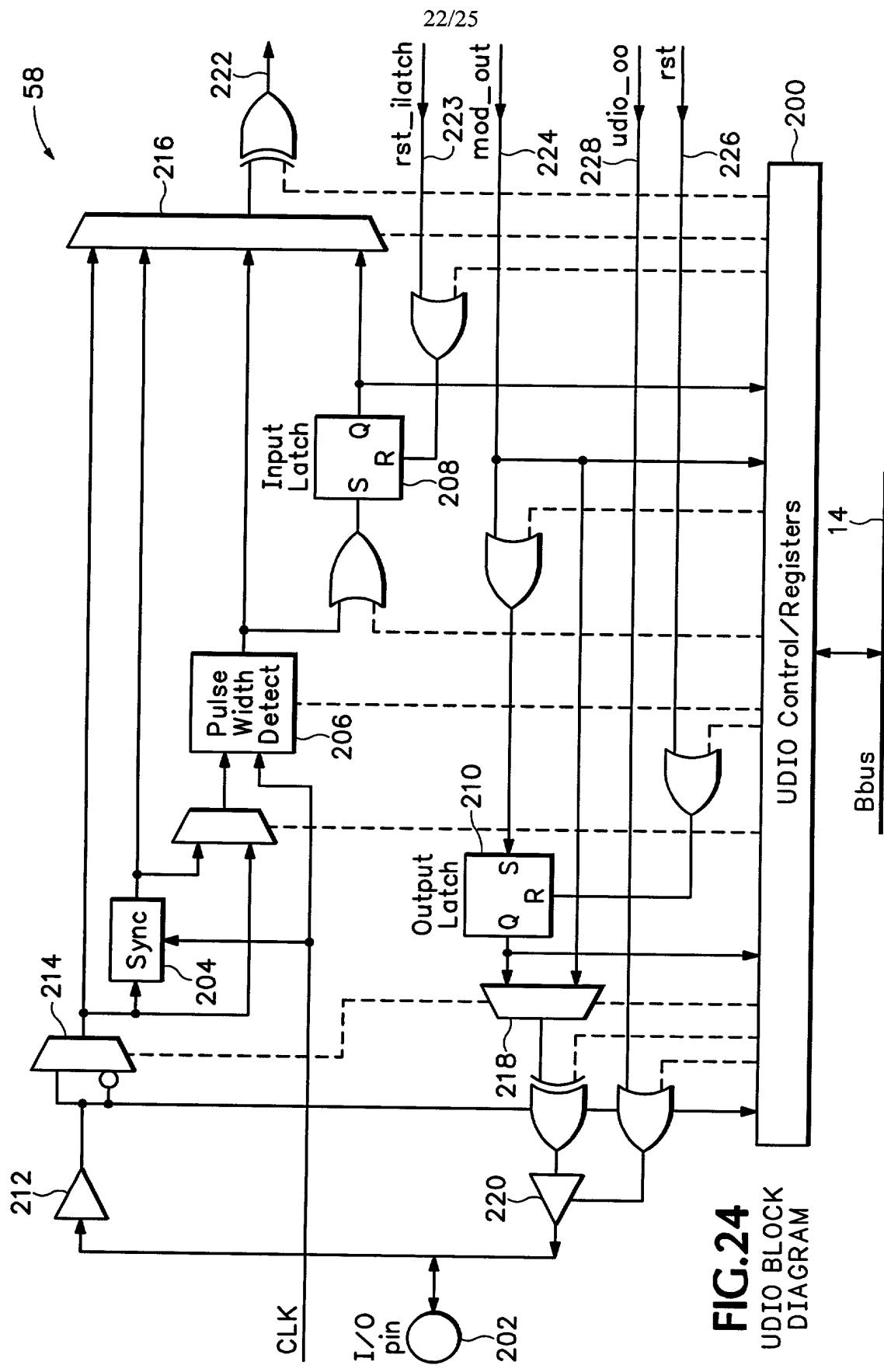


FIG.23
DMA ADDRESS
& CONTROL



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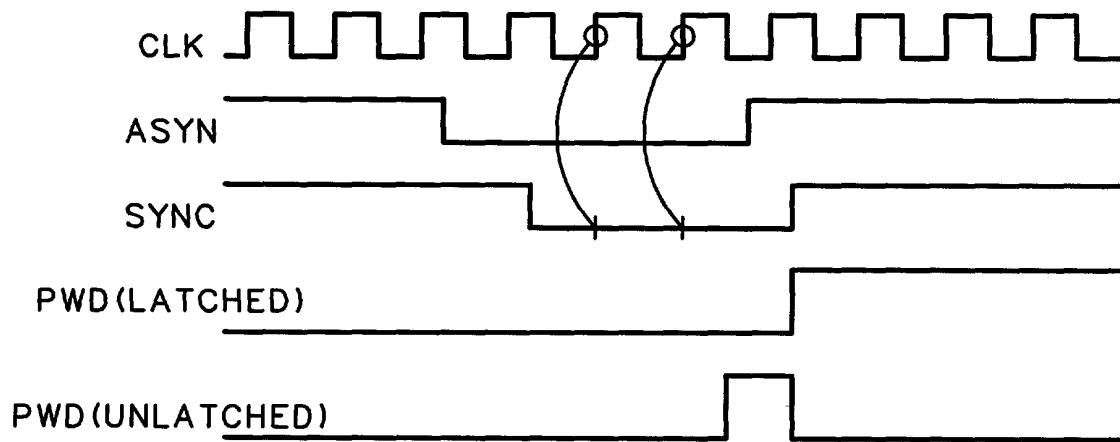


FIG.25

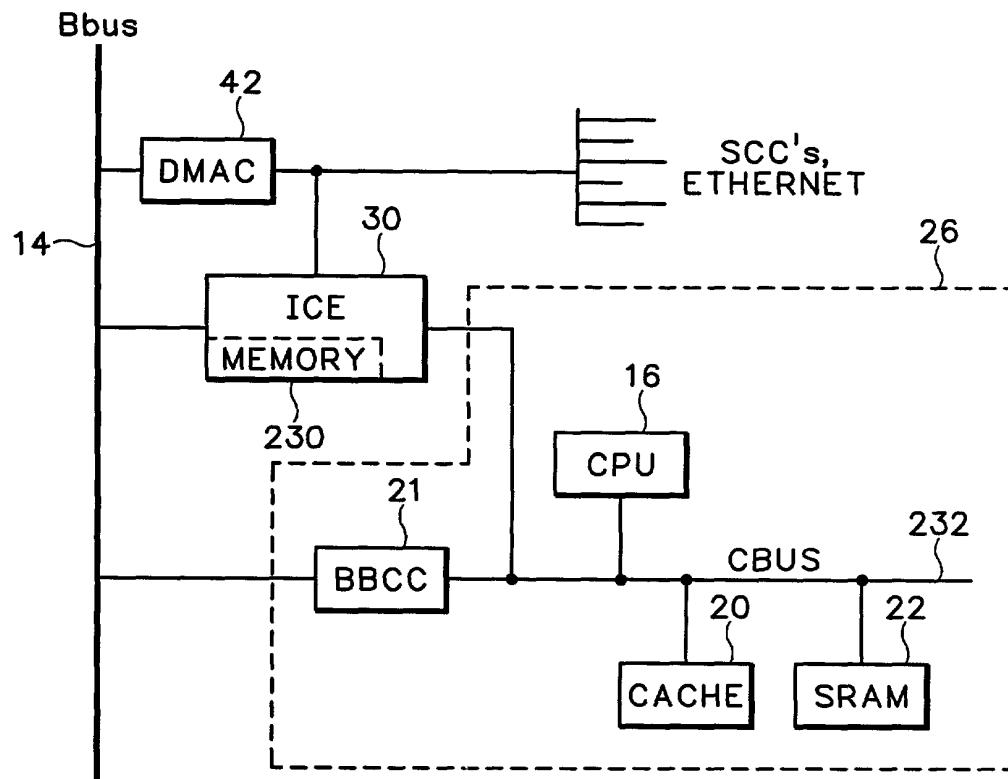


FIG.26

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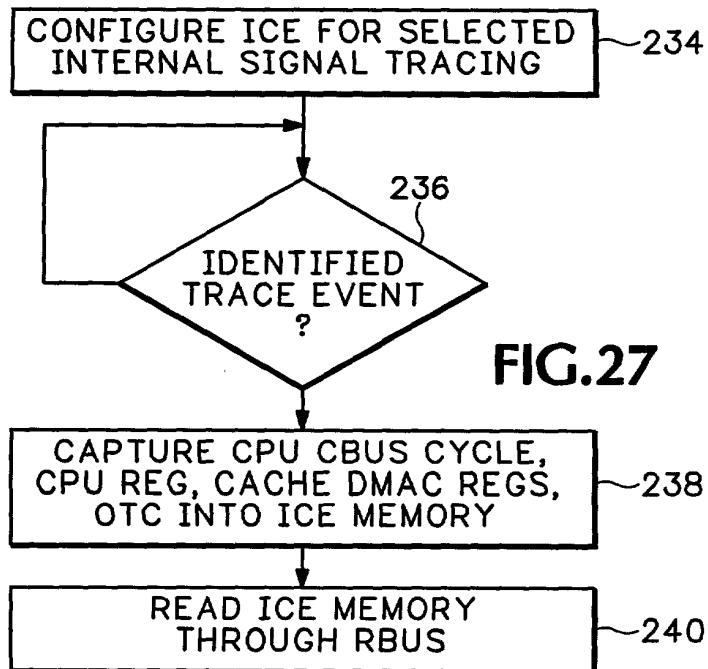


FIG.27

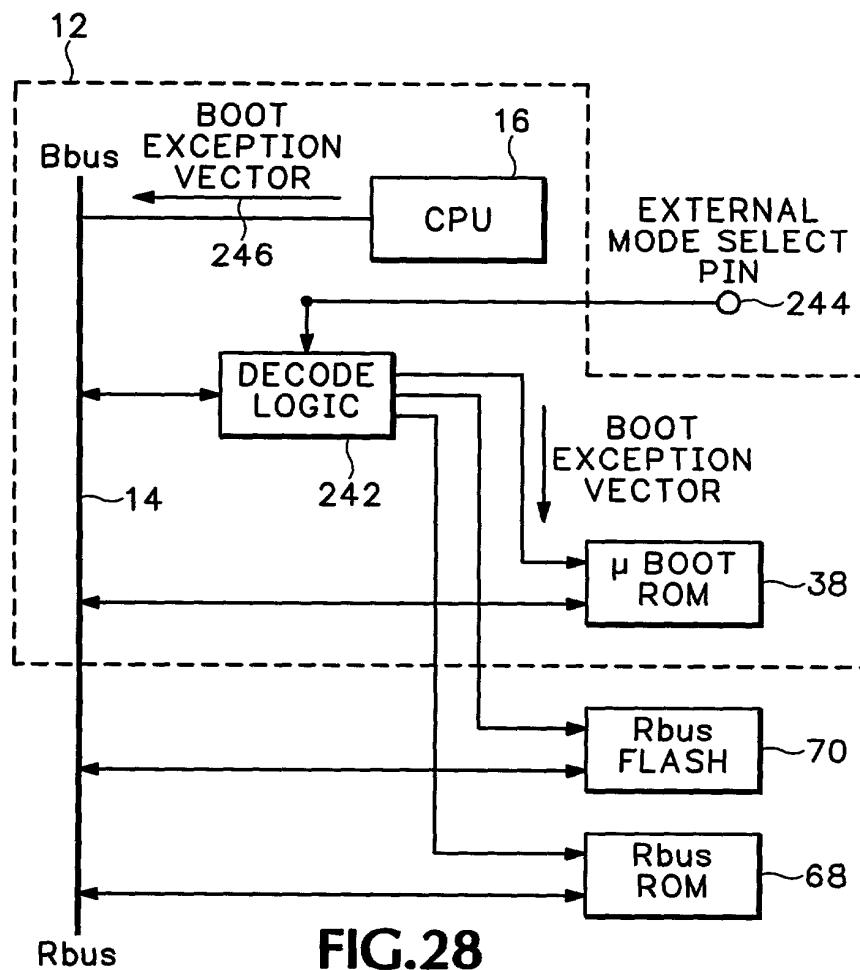


FIG.28

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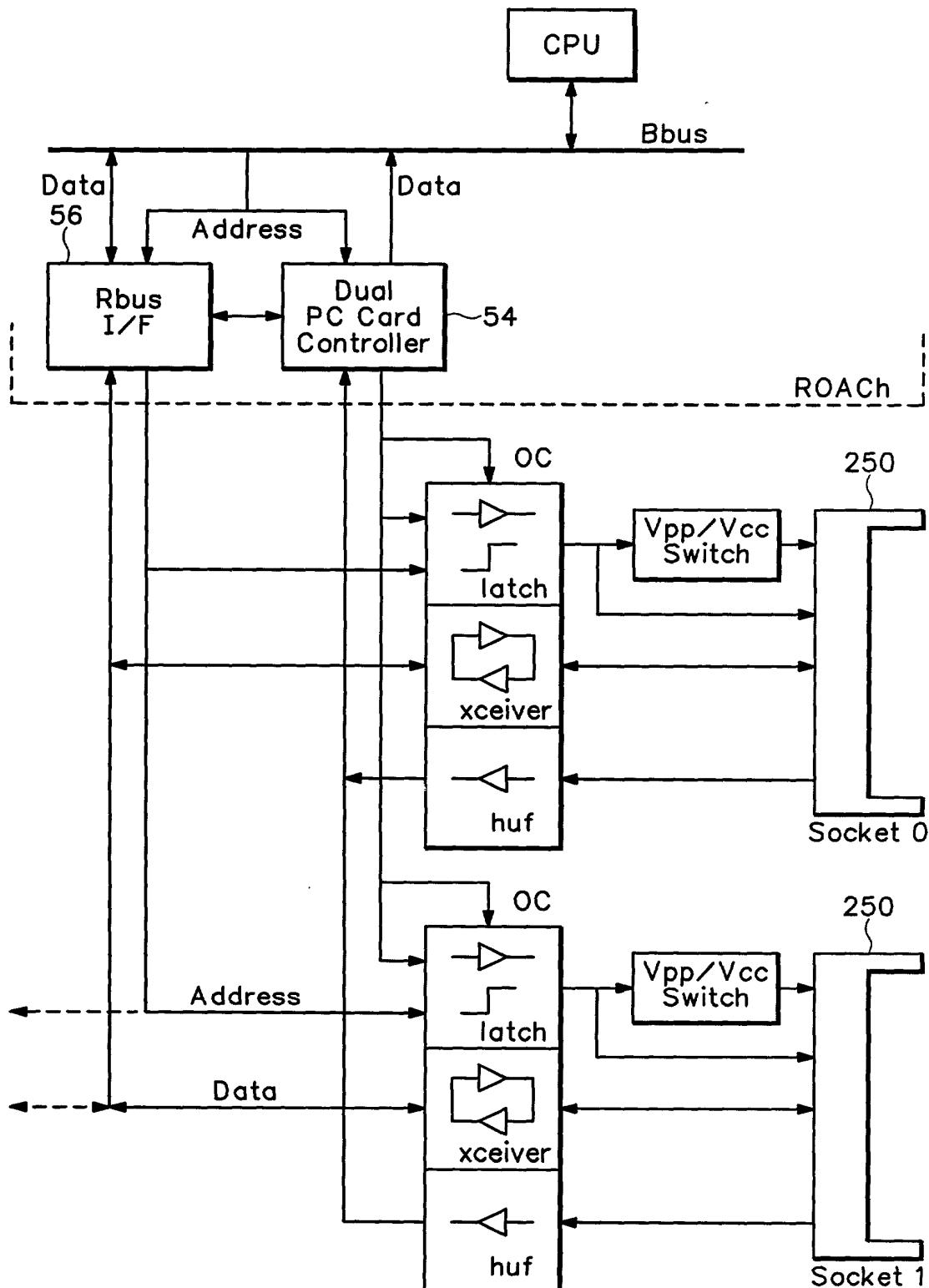


FIG.29
PC CARD INTERFACE